rectangular in configuration; and

a metal layer formed on said first TEOS layer and opposing a corner of said recess.

REMARKS

Claims 1-8 are pending. By this Amendment, claim 1 is amended for clarification purposes only. No new matter is added.

The Office Action rejects claims 1-8 under 35 U.S.C. §103(a) over the Applicants' Admission of Prior Art (AAPA) in view of Hsu et al. (U.S. Patent No. 6,093,640). This rejection is respectfully traversed.

In particular, Applicants assert that it would not have been obvious at the time of the invention to modify the AAPA using the teachings of Hsu to teach or suggest a semiconductor device having a test mark that includes a semiconductor substrate, a first TEOS layer formed on the semiconductor substrate, a second TEOS layer formed on said first TEOS layer, a recess formed in the first and second TEOS layers and a metal layer formed on the first TEOS layer and opposing a corner of the recess, as recited in independent claim 1.

As shown in Figs.14A and 14B, the AAPA device includes test mark having a first insulating layer **22**, i.e. a BPTEOS layer, formed on a substrate **21** with a second insulating layer **23**, i.e., a TEOS layer, formed on the first insulating layer **22**. A square recess **24** is then formed in the first and second insulating layers **22** and **23** to expose the semiconductor substrate **21** below. See, page 2, lines 2-15. Unfortunately, as is depicted in Fig. 13A various cracks **27** can form in the first insulating layer **22** at the corners of the recess **24** when the test mark is exposed to high temperatures because the first insulating layer **22**, having a lower melting point than the second insulating layer **23**, will melt and deform while the second insulating layer **23** maintains

its shape. See, page 2, lines 16-24. The AAPA does not teach or suggest a test mark having a recess formed in a first and second TEOS layers along with a metal layer formed on the first TEOS layer and opposing a corner of the recess, *an issue that the Office Action admits*. See, page 2, last paragraph of the Office Action. Thus, the AAPA does not teach each and every limitation of independent claim 1.

Hsu discloses a box-in-box alignment pattern, including an outer box and an inner box, and method of forming the alignment pattern consistent with damascene technology. See, Abstract. As shown in Figs 3A-5B, the outer box of the alignment pattern **32**, **42** or **52** can be formed in a first insulating layer **30** and subsequently covered with a second insulating layer **35** or **45**, and the inner box **33**, **43** or **53** can be formed on the second insulating layer **35** or **45** to form an alignment mark. See, col. 2, line 66 to col. 3, line 20. Hsu does not teach or suggest a metal layer formed on a first TEOS layer and opposing a corner of a recess.

To the contrary, while the Office Action asserts that "there is an outer metal layer 36 formed outside of the metal layer (32, 42, 52) so that the outer metal layer opposes the corner of the alignment mark", a review of Figs 3a, 3b, 4a, 4b, 5a and 5b shows that in every embodiment connecting line **36** runs parallel to a side of a box **32/33**, **42/43** or **52/53** at an undisclosed distance away from the box **32/33**, **42/43** or **52/53**. Accordingly, the connecting line **36** can not be rationally considered a metal layer formed on the first TEOS layer and opposing a corner of the recess.

While the Office action asserts on page 3, lines 1-3 that Hsu et al. teaches a semiconductor device having a semiconductor substrate, that has an alignment mark configuration on which a metal layer (32, 42 or 52) is formed on an insulating layer and opposing to the corner of the **alignment mark**" {bolded emphasis added}, the Office Action may be equating the

"alignment mark" with the inner box of the alignment mask. Such a construction is not viable as that would require the Office Action to equate the alignment mark of Hsu with the inspection mark of the present invention.

The inspection mark of the present invention is formed for measuring a thickness of a deposited layer, determining overlay accuracy, or measuring a characteristic of a device. See page 1, lines 20-23. Also, the inspection mark is a recess penetrating the first and second insulating layers 2, 3, which is formed after depositing the second insulating layer (TEOS layer) 3. See, Figs. 3F and 3G.

In contrast, the inner box of the Hsu's alignment pattern is formed such that it aligns with the outer box that has already formed in a separate photolithographic step. The alignment tolerances involved are extremely tight. See column 1, lines 18-29. Therefore, Hsu's alignment mark is totally different from the inspection mark in their purposes, the structures, and the forming processes. Accordingly, Hsu does not teach or suggest a metal layer formed on a first TEOS layer and opposing a corner of a recess, as claimed in claim 1.

Thus, Hsu does not provide for the deficiencies of the AAPA.

The Office Action has not established a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations, and there must be some motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the reference teachings. See MPEP §2143, for example. As discussed above, the AAPA and Hsu, individually or in combination, do not teach or suggest a semiconductor device having a recess formed in a first and second TEOS layers and a metal layer formed on the first TEOS layer and opposing a corner of the recess, as recited in independent claim 1.

Furthermore, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the AAPA using the teachings of Hsu. While the Office Action asserts that "it would have been obvious to one of ordinary skill in the art to use a box-in-box configuration as the one taught by Hsu et al. in the area surrounding a test mark area taught by Applicants' admitted prior art for the disclosed intended purpose of improving the identification of the test mark in the wafer patterning" (see, page 3, paragraph 1), this assertion is problematic for several reasons.

First, the asserted motivation of "improving the identification of the test mark in the wafer patterning" is not any motivation to modify the AAPA using the teachings of HSU, but at most a motivation to use the teachings of Hsu alone and unmodified.

Second, Applicants draw attention to the fact that none of the box-in-box alignment marks of Hsu penetrate both insulating layers **30** and **35** to an underlying semiconductor substrate. Accordingly, the AAPA teaches away from the combination of the AAPA and Hsu as the AAPA specifically states that a test mark that does not penetrate both an upper and lower TEOS layer prohibits the measurement of the lower TEOS layer thickness. See, Figs, 15A and 15B, and page 3, lines 6-20 of the Specification.

Third, even if one were motivated to substitute the alignment marks of Hsu for those of the AAPA (an assertion that the Applicants contest), there would still be no motivation to add the connecting wire **36** as the connecting wire **36** has no functional connection whatsoever with the alignment mark. To the contrary, the connecting wire **36** is placed in the same figures merely to demonstrate the compatibility of the Hsu alignment mark with damascene technology and at no time does connecting wire **36** interact with any alignment mark. See, col. 3, lines 3-12 and col. 3, lines 62-66.

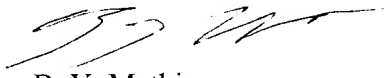
Thus, independent claim 1 defines patentable subject matter. Claims 2-8 define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejection of claims 1-8 under 35 U.S.C. §103(a) is respectfully requested.

For the reasons given, Applicants believe that this application is in condition for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



B. Y. Mathis
Registration No. 44,907

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 BYM/SAB:kap
Date: September 18, 2002
Facsimile: (202) 756-8087

Appendix Showing Claim Changes

Claim 1 has been amended as follows:

1. (Amended) A semiconductor device having a test mark comprising:

a semiconductor substrate;

a first TEOS layer formed on said semiconductor substrate;

a second TEOS layer formed on said first TEOS layer and having a lower fluidity than that of said first TEOS layer at an elevated temperature;

a recess formed in said first and second TEOS layers and exposing the surface of said semiconductor substrate, wherein the horizontal cross-section of said recess is substantially rectangular in configuration; and

a metal layer formed on said first TEOS layer and opposing [to the] a corner of said recess.